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Brief Report

Low dark current P-*InAsSbP*/n-*InAs*/*N*-*InAsSbP*/n^+-*InAs* double heterostructure back-side illuminated photodiodes

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HIGHLIGHTS

- Lowest capacitance of *InAs* heterojunction PD.
- Fast response.
- High detectivity in the 3 μm range.
- BLIP operation at 150 K at 3 μm.
- Flip-chip design.

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ABSTRACT

P-*InAsSbP*/n-*InAs*/N-*InAsSbP*/n^+-*InAs* double heterostructure photodiodes with linear impurity distribution in the space charge region have been fabricated and studied. The photodiodes showed good perspectives for use in low temperature pyrometry as low dark current ($8\cdot10^{-6}$ A/cm^2, $V_{bias} = -0.5$ V, 164 K) and background limited infrared photodetector (BLIP) regime starting from 150 K (2π field of view, $D^*_{3.1\mu m} = 1.4\cdot10^{12}$ cm Hz$^{1/2}$/W) have been demonstrated.

1. Introduction

There is growing interest to photodiodes (PDs) with peak sensitivity around $\lambda = 3$–4 μm for use in thermal imaging [1], low temperature pyrometry [2,3] and in nondispersive infrared (NDIR) analysis of hydrocarbon gases that have fundamental absorption band near the 3.4 μm wavelength. In combination with light emitting diodes (LEDs) with peak emission at 3.4 μm the above large area PDs can be used for low power consumption gas sensors and portable gas analyzers [4] while small (element) area/capacitance PDs are important for recording of fast thermal processes.

In *InAs* based PDs an inversion layer on the surface of the p-type cap layer give rise to leakage current that may be of the same order that the bulk one in small area PDs [5]. This decreases specific detectivity D^* at low temperatures when bulk current is low [5–8]. That's why several passivation techniques including coating with SU-8 photoresist [6–8] and sulphidation treatment [9] have been already suggested in order to suppress surface leakage and to increase the zero bias resistance area product R_0A. On the other hand several publications outlined that creation of *P-InAsSbP/n-InAs/N-InAsSbP* double heterostructures (DH) increases R_0A product and decreases reverse current at high bias with respect to homo *InAs* and single heterojunctions with no *n-InAs/N-InAsSbP* interface (see e.g. [10]).

At the same time several groups reported on deep recombination centers (traps) that assist tunneling [11] and increase a response time [12] in *InAs* based p–n junctions. The authors of [11] stated that the tunnel leakage current is due mostly to the inclined dislocations. The authors of [12,13] reported on deep

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diffusion of *Zn* atoms during the P-*InAsSbP(Zn)* growth onto n-*InAs* with sequential formation of 2–10 μm thick p-*InAs* layer containing electrically active defects [12]. It follows then that to improve the quality of the PDs one have to grow structures with no p-*InAs* layers, e.g. to grow the *P-InAsSbP/n-InAs/N-InAsSbP* DHs with spatial coincidence of p–n junction and heterointerface. Low plasticity of the P-*InAsSbP* quaternary alloy with respect to *InAs* [14] suppresses formation of defects [15] and thus one can expect reduction of leakage current in the P-*InAsSbP* cap layer.

In this paper we present and discuss data on electro-physical and optical characterization of the *P-InAsSbP/n-InAs/N-InAsSbP* DH PDs in the 60–300 K temperature range.

2. Device fabrication and measurements

Wafers were grown at 640–650 °C by the LPE method onto heavily doped n^+-*InAs* (*Sn*) (100) substrates with an electron concentration of $n^+ = (2–3)\cdot10^{18}$ cm^{-3} and contained three epitaxial layers. They represented 2–3 μm thick wide-gap undoped N-*InAsSbP* ($E_g \approx 0.48$ eV, 77 K) confining layer, 3–4 μm thick n-*InAs* active region and 2–3 μm thick wide-gap P-*InAsSbP* (*Zn*) ($E_g \approx 0.48$ eV, 77 K, $P = (2–5)\cdot10^{17}$ cm^{-3}) cap layer. In accordance with formalism and band gap parameters suggested in [16] the energy gap discontinuities constituted to $\Delta E_c = 120$ meV and $\Delta E_v = -30$ meV (300 K); the latter form shallow potential wells at an isotype N-*InAsSbP/n-InAs* interface (see Fig. 1). The photoluminescence spectrum of the narrow gap layer measured at 77 K in a reflection mode showed an emission peak at 0.41 eV, which is a common value for the undoped n^0-*InAs;* room temperature electroluminescence peaked at 0.36 eV typical for LEDs with n^0-*InAs* active layer as well. The latter suggests lack of P-*InAsSbP*/p-*InAs* heterojunction in our samples as the above Type II junction usually causes high radiative recombination rate of electron-hole pairs localized at shallow quantum wells at the P-*InAsSbP*/p-*InAs* interface with subsequent electroluminescent peak emission formation at 0.32 eV (300 K) [13]. It is worth mentioning that close proximity of p–n junction and *InAsSbP*/*InAs* interface has been already confirmed by the Atomic Force Microscopy (AFM) measurements in single P-*InAsSbP*/n-*InAs* heterostructure analogs grown by close procedure [17] and by recent AFM measurements to be published shortly.

Standard optical photolithography and wet chemical etching processes developed by Ioffe Institute together with IoffeLED, Ltd. have been implemented to obtain two types of rectangular PD chips with circular mesa ($d_1^m = 90$ μm and $d_2^m = 260$ μm) as high as 15 μm. Broad reflective Ag-based anode onto the P-*InAsSbP* cap layer and *Cr–Au–Ni–Au* cathode onto the n^+-*InAs* substrate material were formed by evaporation in vacuum; together with Au wires they provided electrical connection to external circuits. Backside illumination (BSI) through a 110 μm thick substrate without shadowing by electrical contacts has been organized. PD chips were mounted into TO-18 cases; no special passivation technique has been implemented.

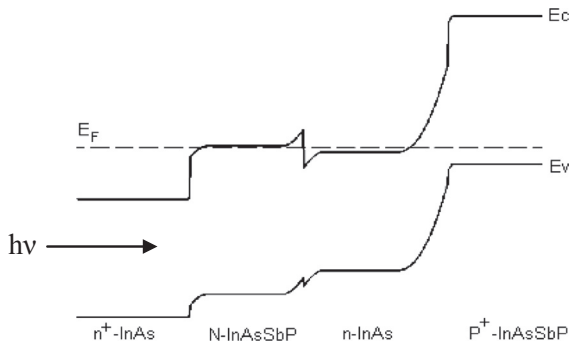

Fig. 1. Energy band-gap schematic of the P-*InAsSbP*/n-*InAs*/N-*InAsSbP*/n^+-*InAs* DH.

Current–voltage (*I–V*) characteristics were measured in the range of $I = 10^{-14}$–10^{-3} A under dark or illuminated conditions at the CW mode using sub-femtoampere SourceMeter Keithley 6430 equipped with a remote preamplifier. $1/R_o$ (the derivative of the experimental *I–V* dependence near $V = 0$) was obtained via direct measurements at $|V_{bias}| < 5$ mV. The sample was mounted in the Closed Cycle Refrigerator CCS-450 DLTS (Janis). Optical source with $\lambda = 3$ μm was a light emitting diode LED30Sr (IoffeLED, Ltd.) with an immersion lens. Capacitance–voltage (*C–V*) characteristics were measured with E4980A LCR meter (KEYSIGHT Technologies) in the modulation frequency range of $f = 0.1$–2000 kHz.

Current sensitivity at maximum ($S_{\lambda max}$) was estimated with a Black Body model at 573 K using the sample with 260 μm wide circular mesa that provided minimal uncertainty in the incoming radiation flux. Relative S_λ spectra were measured with Globar as a light source.

3. Results and discussion

Fig. 2 presents typical temperature dependent *I–V* characteristics. Values of the current below $5\cdot10^{-14}$ A are obviously uncertain because of noise. Low temperature reverse bias (RB) *I–V* characteristics at $|V_{bias}| > 0.4$ V most likely indicate leakage current but not an avalanche multiplication. This conclusion is supported by the fact that the 60 K photocurrent induced by the LED30Sr illumination was almost independent on V_{bias} indicating low avalanche multiplication probability for holes in n-*InAs*. The latter agrees with the recent evaluation of low value of the hole ionization coefficient in *InAs* [6–8].

The 296 K I^{FB}–*V* data as well as data for some other temperatures deviated from exponent at high currents probably due to series resistance impact. The ideality factor β derived from the modified Shockley formula ($I = I_o[\exp(eV/\beta kT) - 1]$) fitting had negligible dependence on temperature and was close to unity (see insert in Fig. 2) suggesting diffusion current domination in the whole 80–296 K temperature range.

Fig. 3 shows temperature variation of the R_oA product measured at $|V_{bias}| < 0.005$ V ($115 < T < 300$ K) and that simulated as $R_0A = A\beta kT/eI_o$ (FB fit, $T < 115$ K). Fig. 3 presents also the simulated detectivity $D^*_{\lambda max}$ values evaluated for thermal noise domination ($D^*_{\lambda max} = S_{\lambda max}\sqrt{R_oA/4kT}$, $S_{\lambda max}$ –current sensitivity at maximum). It follows from the Arrhenius plot in Fig. 3 that the activation energy of the temperature dependence of the R_oA product ($E = 0.25$ eV) is quite close to the *InAs* energy gap value. It is worth

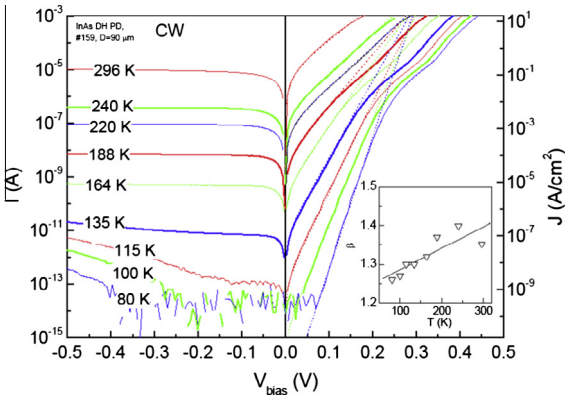

Fig. 2. Temperature-dependent semilog *I–V* characteristics of *InAs* DH diode with $d = 90$ μm. In the insert – ideality factor (β) vs temperature.

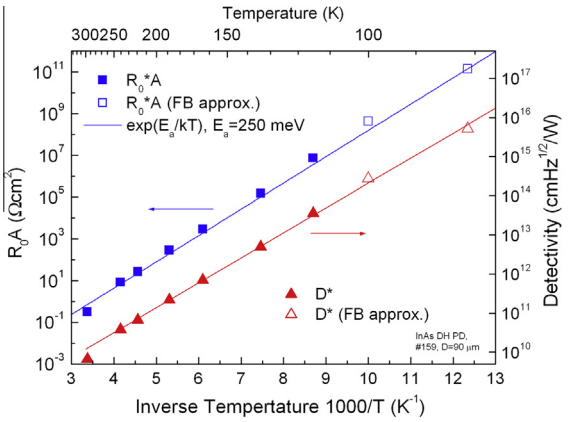

Fig. 3. Temperature dependence of the R_oA product derived from direct measurements (filled squares, left scale) and from simulation (FB data, empty squares, left scale) vs temperature. Right scale is for the detectivity at maximum.

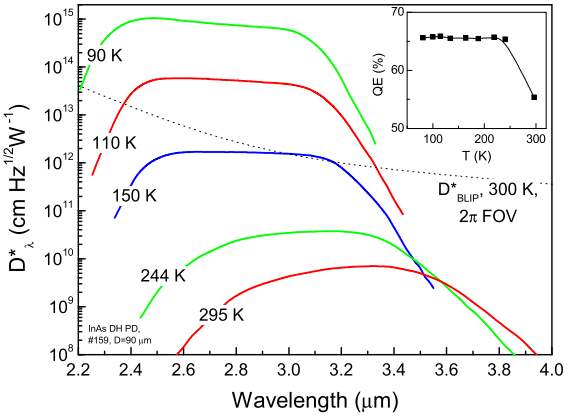

Fig. 4. Spectra of detectivity D^*_λ at different temperatures for the 90 μm wide PD. The insert shows quantum efficiency QE at λ_{max} vs temperature for the 260 μm wide PD.

to note that the R_oA value grows faster than the exp ($E_g/2kT$) on temperature decrease; this together with low β value means that influence of tunneling current is negligible.

Spectra of D^*_λ at several temperatures are presented in Fig. 4. The quantum efficiency QE at peak wavelength λ_{max} does not depend on temperature in the range from 80 K to 250 K, and drops as temperature increases from 250 up to 300 K (see the insert in Fig. 4). The latter can be explained by both transparency reduction of the n$^+$-*InAs* substrate due to the breakdown of electron degeneration in the conduction band [18,19] and by minority carrier diffusion length (L_p) decrease at elevated temperatures. Indeed, simulated reduction in 110 μm thick n$^+$-*InAs* transparency using data in [19] amounts to 6–9% at PD peak wavelength in the 83–300 K interval, whereas sensitivity/collection efficiency drop at maximum in nominally similar front surface illuminated P-*InAsSbP*/n-*InAs* single heterostructures was of same above value as well [17]. At temperature above 134 K the $D^*_{\lambda max}$ values are close to that of "broad area" PD in [10] and are several orders higher than in p–i–n junction PDs [5,8] and n–B–n PDs [20]. As a result the BLIP regime temperature was achieved at temperature as high as 150 K for the 2π FOV and λ_{max} = 3.1 μm.

In contrast to all previous *InAs*/*InAsSbP* PDs with an abrupt p–n junction (see e.g. [11,12]) capacitance of our PDs varied as ($1/C^3$)–V_{bias} (see Fig. 5b) suggesting linear impurity distribution within the space charge region. As a result the fabricated PDs exhibited as low unit area capacitance as $C_o/A = 9.4\cdot10^{-8}$ and $2.4\cdot10^{-8}$ F cm^{-2} at room temperature and 80 K correspondingly. To the best of our knowledge the above numbers are less than any data published on *InAs* heterostructure PDs and thus this makes good promises for small PD response time expectations as $\tau = RC_o = 300$ and 75 ps for the 90 μm wide device and standard load of 50 Ω.

The above conclusion on limited influence of deep centers on transport and recombination processes is also supported by an independence of zero bias capacitance C_o on a modulation frequency (see Fig. 5c) that normally states absence of electrically active deep levels. Previous investigations of heterostructures that contained both n-*InAs* and p-*InAs* layers outlined existence of defects solely in p-*InAs*, defects and their electrical activity in n-*InAs* layer were ignored/not traced. An independence of the ($1/C^3$)–V_{bias} slope on temperature confirms independence of charge

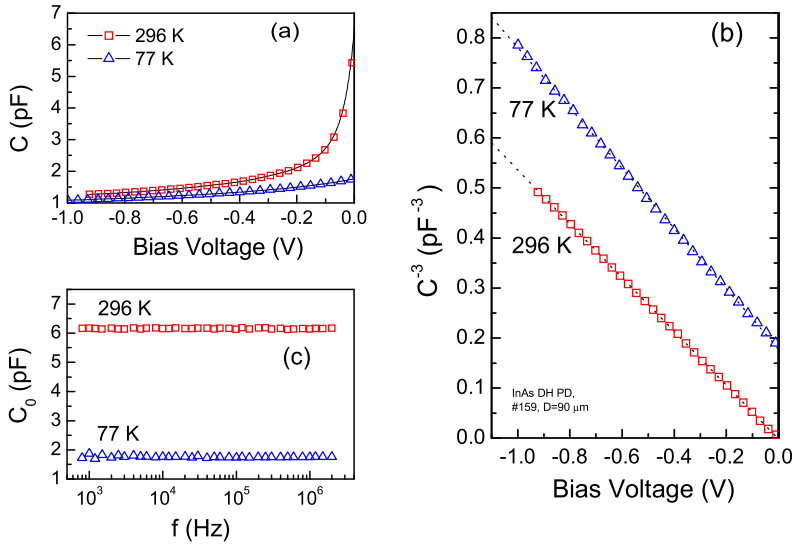

Fig. 5. C–V (a) and ($1/C^3$)–V (b) characteristics at 77 and 300 K at f = 2 MHz, capacitance at V_{bias} = 0 V vs frequency at 300 K and 77 K (c).

carrier concentration – feature not suitable for semiconductor with sufficient amount of deep levels in the forbidden energy gap. The reason for the C_o temperature dependence at zero and small bias was the energy gap and corresponding potential barrier variation as followed from analysis of the *C–V* characteristics: the calculated concentration of charge carriers was the same for 77 and 300 K; free carrier concentration in the vicinity of the p–n junction ranged from $3{\cdot}10^{15}$ to $6{\cdot}10^{15}$ cm^{-3}. These values are very close to the intrinsic carrier concentration in n-*InAs* at 300 K.

4. Conclusion

Low dark current ($8{\cdot}10^{-6}$ A/cm^2, $V_{bias} = -0.5$ V, 164 K) P-*InAsSbP*/n-*InAs*/N-*InAsSbP*/n^+-*InAs* double heterostructure photodiodes exhibited BLIP operation below 150 K (2π FOV) with negligible influence of generation–recombination and tunneling currents in the 80–300 K temperature interval. These features most likely arose from absence of p-*InAs* layer and corresponding electrically active defects and low defect density in n-*InAs* and P (N)-*InAsSbP* layers. Low unit area capacity ($2.4{\cdot}10^{-8}$ F cm^{-2}, 80 K) in the above "defect free" *InAsSbP*/*InAs* PDs with linear impurity distribution in the p–n junction makes promises for fabrication in future efficient mid-IR detectors with small response time.

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